Preliminary

SANYO Semiconductors
DATA SHEET

# CCB(Computer Control Bus) IC I/F Serial Bus Format

## Overview

This Computer Control Bus (CCB) is a bus format that is designed to ensure that communication in a system configured with a multiple number of ICs is achieved reliably and economically. It is designed for communication between ICs in equipment and not for communication between products requiring long lines.

## Features

The CCB is a single master system, which obviates the need for complex arbitration processing. This reduces the hardware load significantly, enabling the construction of extremely economical systems. Furthermore, many and varied groups of devices including tuners, electronic volumes, digital signal processors for audio application and display drivers are provided to support a broad spectrum of needs. Using software or serial I/O facilities, the CCB can easily interface with many different kinds of controllers so that no special hardware is required.

- CCB is a registered trademark of SANYO Electric Co., Ltd.
- CCB is SANYO Semiconductor's original bus format. All bus addresses are managed by SANYO Semiconductor for this format.



SANYO Semiconductor Co., Ltd.
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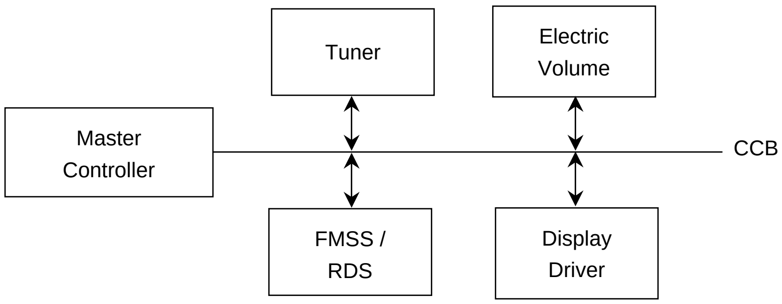
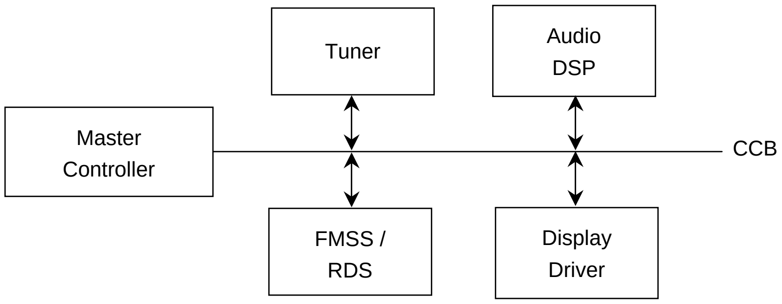
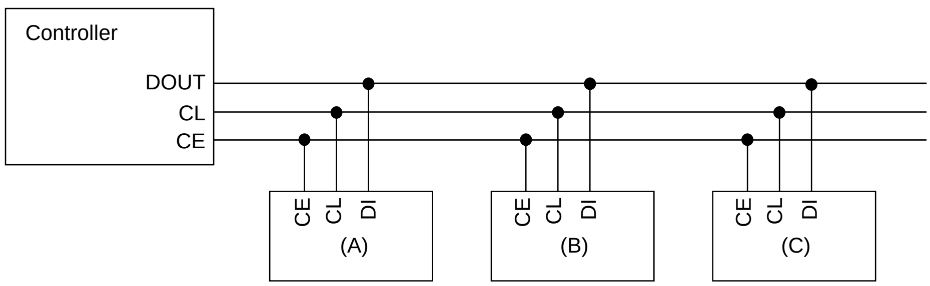



## Configuration of Serial Data Communication

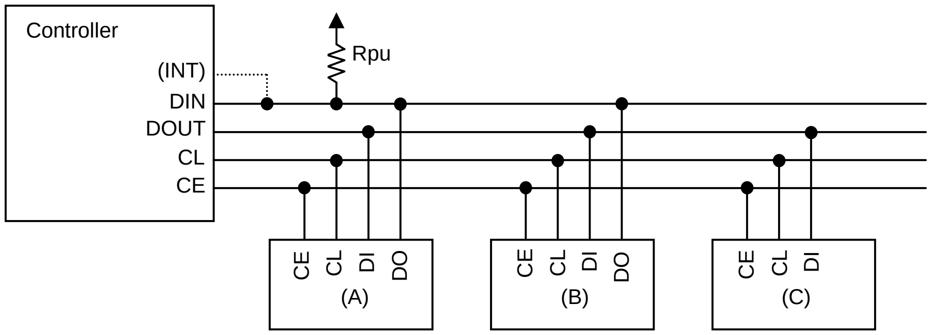
CCB format based communication between the controller and the peripheral ICs can be achieved in two ways: unidirectional communication (one-way communication between the controller and peripheral ICs) or bidirectional communication (two-way communication between the controller and peripheral ICs and two-way communication between the peripheral ICs).
Unidirectional communication is configured with the three lines of the chip enable signal CE, synchronized clock signal CL and input data signal DI, whereas bidirectional communication is configured with the four lines of the chip enable signal CE, synchronized clock signal CL, input data signal DI and output data signal DO. In recent years, ICs with a new means of bidirectional communication, consisting of the three lines of the chip enable signal CE, synchronized clock signal CL and input/output data signal DI/DO, have also being developed.

1. Unidirectional communication (one-way communication between the controller and peripheral ICs)
   Configured with the three lines of the chip enable signal CE, synchronized clock signal CL and input data signal DI

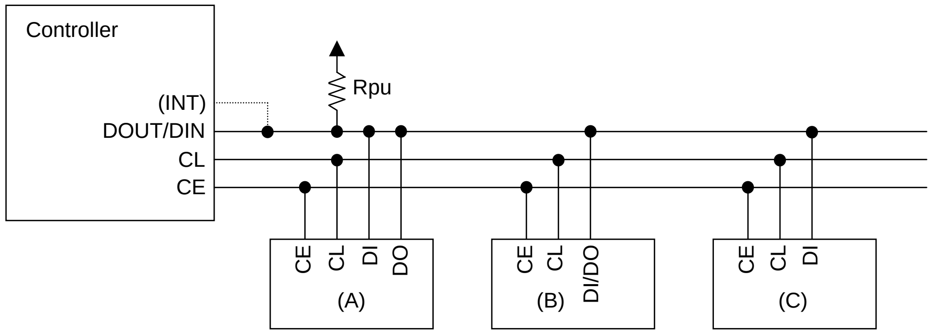



2. Bidirectional communication (two-way communication between the controller and peripheral ICs)

<2-1> Configured with the four lines of the chip enable signal CE, synchronized clock signal CL, input data signal DI and output data signal DO



<2-2> Configured with the three lines of the chip enable signal CE, synchronized clock signal CL and input/output data signal DI/DO (This means of bidirectional communication is new for the CCB, and ICs featuring this function must be employed in order to use this communication method.)




[Note] Rpu: Pull-up resistor
(INT): Input port for detecting data read request signal

## Serial Data Communication Format

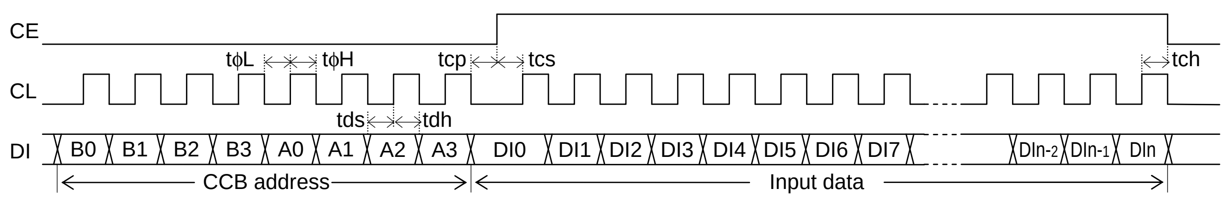
Under the CCB format, when data is to be sent from the controller to the peripheral ICs, it is sent by the following series of operations. The controller transfers the CCB addresses B0 to B3 and A0 to A3 while the chip enable signal CE is low. After all the addresses have been transferred, the CE signal level is switched from low to high, and while this signal is high, the data DI0 to DIn (input data) required by the peripheral ICs is transferred. The CE signal level is then switched from high to low. In addition, the CCB addresses and input data to be sent from the controller are imported into the peripheral ICs by the rising edge of the CL signal.

On the other hand, when data is to be received by the controller from the peripheral ICs, it is received by the following series of operations. The controller transfers the CCB addresses B0 to B3 and A0 to A3 while the chip enable signal CE is low. After all the addresses have been transferred, the CE signal level is switched from low to high, and while this signal is high, the data DO0 to DOm (output data) is read from the peripheral ICs. CE signal level is then switched from high to low. In addition, since the CCB addresses to be sent from the controller are imported into the peripheral ICs by the rising edge of the CL signal, and the output data to be received by the controller is output from the peripheral ICs in synchronization with the falling edge of the CL signal, the controller can import the output data DO0 to DOm at the rising edge of the CL signal.

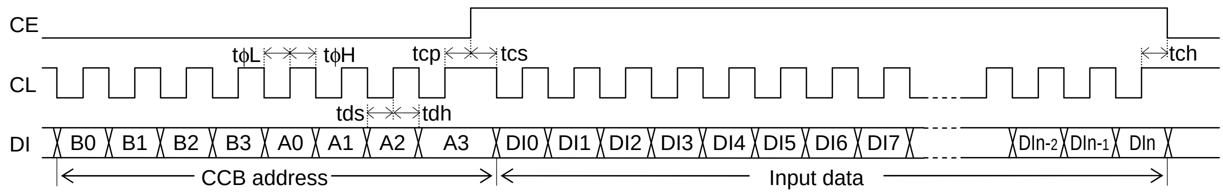
As a basic rule, the CCB addresses have a bit width of 8 bits, and the data has a bit width that is a multiple of 8 (8 × a bit width where "a" is a natural number). However, there are 4-bit CCB address groups among the CCB address groups so, in this case, dummy data must be added to the CCB addresses B0 to B3.

1. Unidirectional communication format (consisting of the 3 lines of CE, CL, and DI)

(1) When communication is stopped with CL at the low level



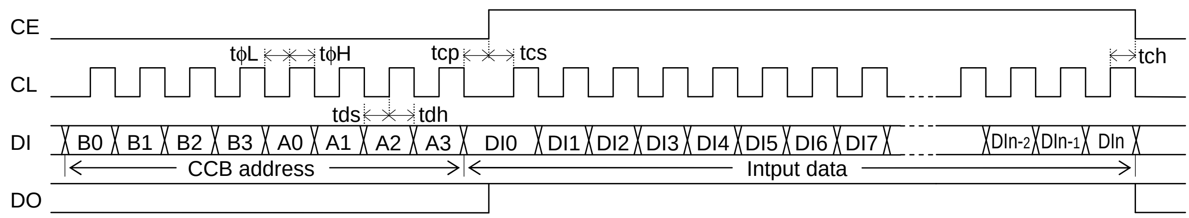
(2) When communication is stopped with CL at the high level



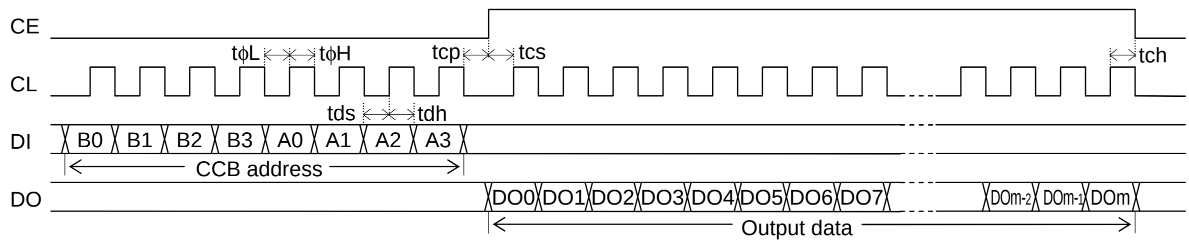

[Note]
tds: Data setup time
tdh: Data hold time
tcp: CE wait time
tcs: CE setup time
tch: CE hold time
tϕH: High level clock pulse width
tϕL: Low level clock pulse width

2. Bidirectional communication format
<2-1> Bidirectional communication format (consisting of the 4 lines of CE, CL, DI, and DO)

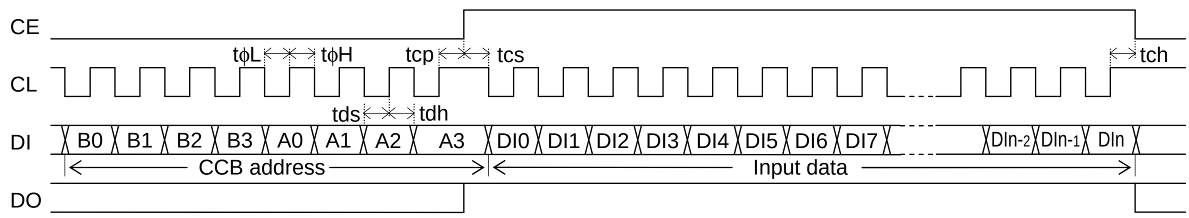
(1) When communication is stopped with CL at the low level
①When the controller sends the data to the peripheral ICs (serial data input)



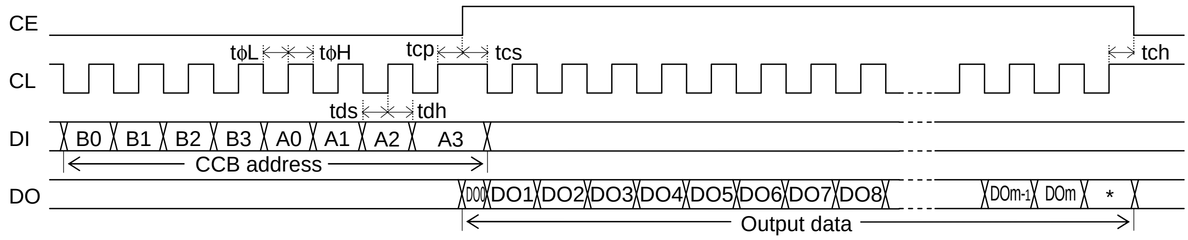

②When the controller receives the data from the peripheral ICs (serial data output)




(2) When communication is stopped with CL at the high level
①When the controller sends the data to the peripheral ICs (serial data input)



②When the controller receives the data from the peripheral ICs (serial data output)




*: don’t care

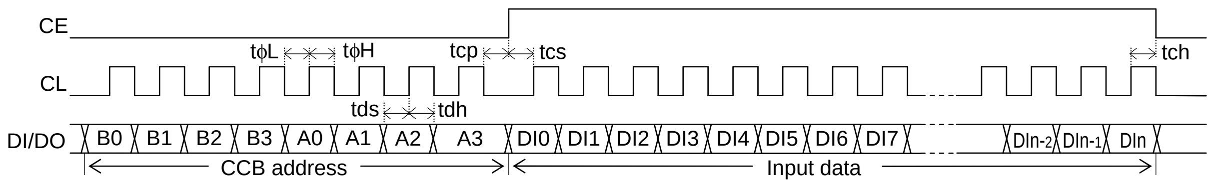
[Note] The output data DO0 to DOm is shifted by 1 bit between ① when communication is stopped with CL at the low level and ② when communication is stopped with CL at the high level, so that use of the output data DO0 is not recommended. Furthermore, when using output data DO0, the status of the DO signal immediately after the CE signal level has changed from low to high must be detected.

<2-2> Bidirectional communication format (consisting of the 3 lines of CE, CL, and DI/DO)

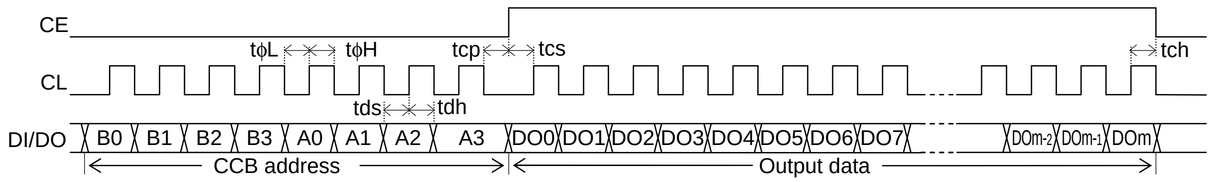
(This means of bidirectional communication is new for the CCB, and devices featuring this function must be employed in order to use this communication method.)

(1) When communication is stopped with CL at the low level

①When the controller sends the data to the peripheral ICs (serial data input)

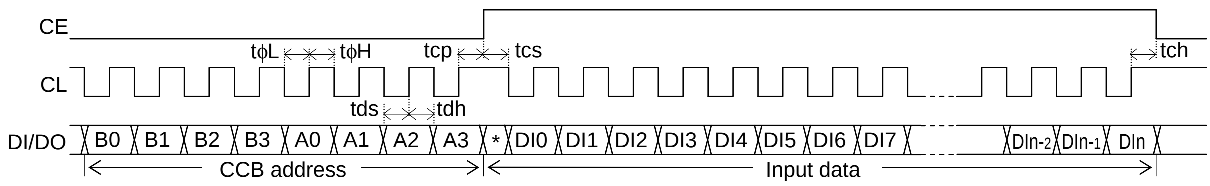



②When the controller receives the data from the peripheral ICs (serial data output)

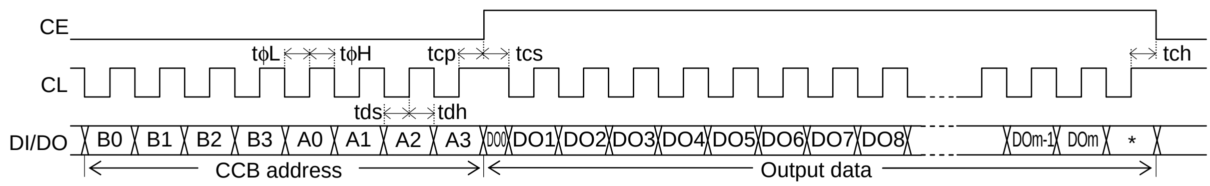



(2) When communication is stopped with CL at the high level

①When the controller sends the data to the peripheral ICs (serial data input)




②When the controller receives the data from the peripheral ICs (serial data output)



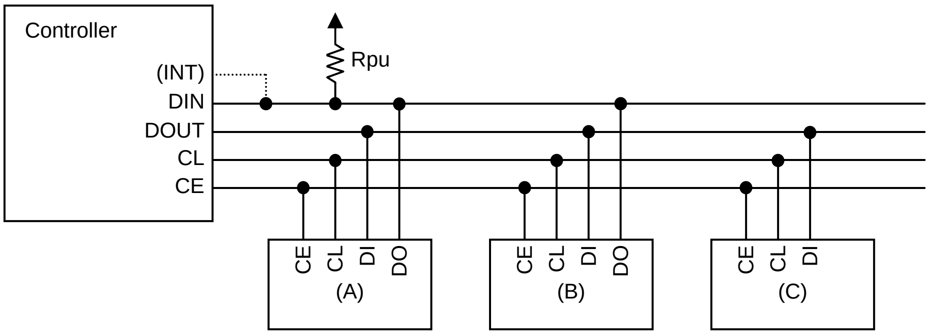

*:don’t care

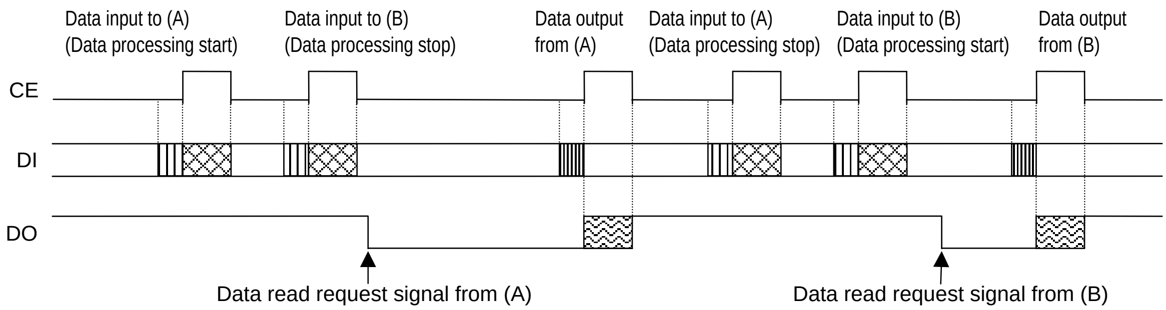
[Note] The output data DO0 to DOm is shifted by 1 bit between ① when communication is stopped with CL at the low level and ② when communication is stopped with CL at the high level so that use of the output data DO0 is not recommended. Furthermore, when using output data DO0, the status of the DI/DO signal immediately after the CE signal level has changed from low to high must be detected.

## Concerning the Data Read Request Signal and Serial Data Communication

Also provided with the CCB format is a function that passes the data read request signal along the output data signal DO line and outputs it to the controller for cases in which data that has been processed by the peripheral ICs is to be output to the controller, or where the peripheral ICs request that the serial data be sent from the controller, for instance. In addition, when serial data communication is not performed between the controller and peripheral ICs (when the chip enable signal CE level is low), the data read request signal is output by setting the output data signal DO to the low level, and when the controller detects this data read request signal, it proceeds to read the data as shown below for the peripheral ICs.

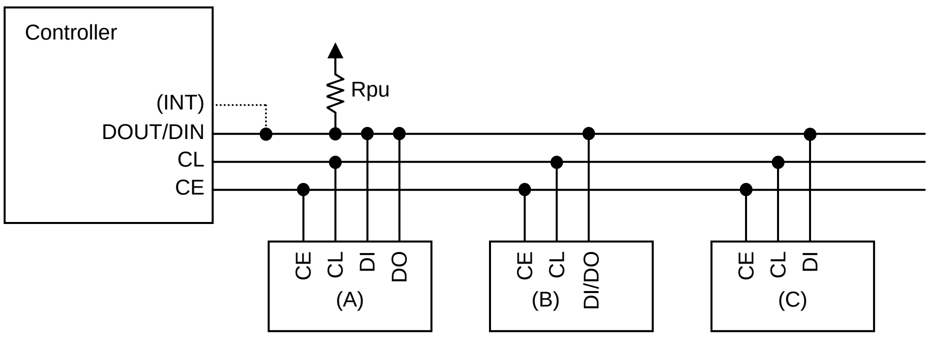
<1> Bidirectional communication format (consisting of the 4 lines of CE, CL, DI, and DO)

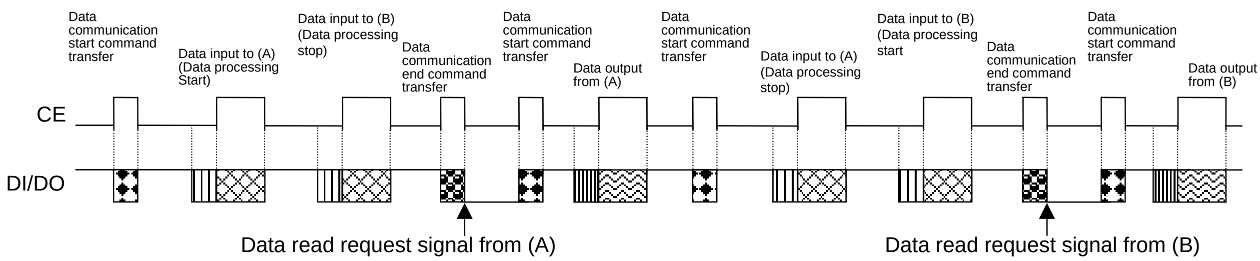



<2> Bidirectional communication format (consisting of the 3 lines of CE, CL, and DI/DO)

(This means of bidirectional communication is new for the CCB, and ICs featuring this function must be employed in order to use this communication method.)



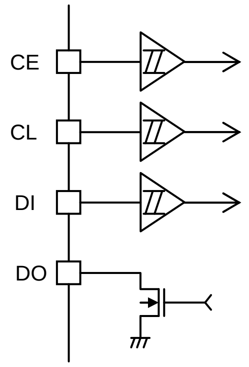




[Note] When serial data communication is to be performed, the data communication start command must be transferred. When the data read request signal (DO = low) is to be detected, the data communication end command must be transferred. For further details on the data communication start and end commands, refer to the individual specification document of each device.

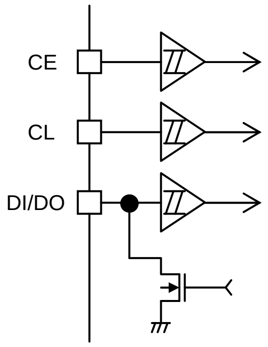
## Concerning the Interface Pins Connected to the Controller

The chip enable signal input pin CE, synchronized clock signal input pin CL and input data signal input pin DI of the peripheral ICs are input pins that are configured using schmitt circuits, among others. The output data signal output pin DO is an output pin that is configured with an open-drain N-channel transistor, for instance, and a pull-up resistor is required. The electrical characteristics of these pins are as shown below. (For further details on the electrical characteristics of these pins, refer to the individual catalog and delivery specification documents of each device.)

<1> Equivalent circuits of CE, CL, DI and DO pins




<2> Equivalent circuits of CE, CL, and DI/DO pins




1. Example of electrical characteristics of CE, CL and DI input pins

[Example 1] $V_{IN}$ = –0.3 to +4.2V or $V_{IN}$ = –0.3 to +6.5V

In this example, the IC can apply a voltage to the CE, CL and DI pins regardless of supply voltage $V_{DD}$. Even when no power is supplied to the IC, voltages can be applied to the CE, CL and DI pins. However, care is required since the maximum voltage that can be applied differs from one IC to another. If the specifications give $V_{IN}$ = –0.3 to +4.2V, for instance, a 3.3V voltage can be applied regardless of supply voltage $V_{DD}$, but a 5V voltage cannot be applied. (If the specifications give $V_{IN}$ = –0.3 to +6.5V, a 5V voltage can be applied regardless of supply voltage $V_{DD}$.)

[Example 2] $V_{IN}$ = –0.3 to +6.5V (provided that supply voltage $V_{DD}$ = 3.0 to 3.6V)

In this example, when a 3.0 to 3.6V voltage is supplied to supply voltage $V_{DD}$, a voltage can be applied to the CE, CL and DI pins regardless of the supply voltage $V_{DD}$. In other words, if a 3.0 to 3.6V voltage is being supplied to supply voltage $V_{DD}$ of the IC, it is possible to apply a 3.3V or 5V voltage to the CE, CL and DI pins.

[Example 3] $V_{IN}$ = –0.3 to $V_{DD}$ +0.3V

In this example, the IC cannot apply a voltage in excess of supply voltage $V_{DD}$ to the CE, CL and DI pins, and a voltage equivalent to supply voltage $V_{DD}$ or less can be supplied to these pins while power is being supplied to the IC. If no power is supplied to the device, supply voltage $V_{DD}$ is normally the same as $V_{SS}$ (GND) so that the CE, CL and DI pins must have the same potential as $V_{SS}$ (GND).

2. Example of electrical characteristics of DO output pin

[Example 1] $V_{OUT}$ = –0.3 to +4.2V or $V_{OUT}$ = –0.3 to +6.5V

In this example, the IC can apply a pull-up voltage to the DO pin regardless of supply voltage $V_{DD}$. Even when no power is being supplied to the IC, a pull-up voltage can be applied to the DO pin. However, care is required since the maximum pull-up voltage that can be applied differs from one IC to another. If the specifications give $V_{OUT}$ = –0.3 to +4.2V, for instance, a 3.3V pull-up voltage can be applied regardless of supply voltage $V_{DD}$, but a 5V voltage cannot be applied. (If the specifications give $V_{OUT}$ = –0.3 to +6.5V, a 5V pull-up voltage can be applied regardless of supply voltage $V_{DD}$.)

[Example 2] $V_{OUT}$ = –0.3 to $V_{DD}$ +0.3V

In this example, the IC cannot apply a pull-up voltage in excess of supply voltage $V_{DD}$ to the DO pin, and a pull-up voltage equivalent to supply voltage $V_{DD}$ or less can be applied to this pin while power is being supplied to the IC. If no power is supplied to the IC, the pull-up voltage of the DO pin must be set to off or steps must be taken to isolate the DO pin from the pull-up power supply, for instance.

## CCB Address Group

1. 8-bit address group

| CCB address | | | | | | | | | Device name (IC name) |
|---|---|---|---|---|---|---|---|---|---|
| Binary display LSB | | | | | | | MSB | Hex display | |
| B0 | B1 | B2 | B3 | A0 | A1 | A2 | A3 | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 | Used for data communication start and end commands |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 10 | |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 11 | |
| ↓ | | | | | | | | ↓ | ↓ |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1F | |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 20 | |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 21 | |
| ↓ | | | | | | | | ↓ | ↓ |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 28 | LV23xxx series, LV25xxx series (Tuner) |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 29 | LV23xxx series, LV25xxx series (Tuner) |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 2A | LV23xxx series, LV25xxx series (Tuner) |
| ↓ | | | | | | | | ↓ | ↓ |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 2F | |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 30 | |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 31 | |
| ↓ | | | | | | | | ↓ | ↓ |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 3F | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 40 | LC758xx series (LCD display driver) |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 41 | LC758xx series (LCD display driver) |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 42 | LC758xx series (LCD display driver) |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 43 | LC758xx series (LCD display driver) |
| ↓ | | | | | | | | ↓ | ↓ |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 4F | LC758xx series (LCD display driver) |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 50 | |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 51 | |
| ↓ | | | | | | | | ↓ | ↓ |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 5F | |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 60 | |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 61 | |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 62 | LC75700 (Key scan IC) |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 63 | LC75700 (Key scan IC) |
| ↓ | | | | | | | | ↓ | ↓ |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 6A | LC72720, LC72722 (RDS) |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 6B | LC72720, LC72722 (RDS) |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 6C | LC72720, LC72722 (RDS) |
| ↓ | | | | | | | | ↓ | ↓ |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 6F | |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 70 | |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 71 | |
| ↓ | | | | | | | | ↓ | ↓ |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 7F | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 80 | |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 81 | LC754x series (Electronic volume) |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 82 | LC753x series (Electronic volume) |
| ↓ | | | | | | | | ↓ | ↓ |

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| CCB address | | | | | | | | | Device name (IC name) |
|---|---|---|---|---|---|---|---|---|---|
| Binary display LSB … MSB | | | | | | | | Hex display | |
| B0 | B1 | B2 | B3 | A0 | A1 | A2 | A3 | | |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 8E | LC757xx series (VFD display driver) |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 8F | LC757xx series (VFD display driver) |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 90 | |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 91 | |
| | | | ↓ | | | | | ↓ | ↓ |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 9F | |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | A0 | |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | A1 | |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | A2 | LC758xx series (LCD display driver) |
| | | | ↓ | | | | | ↓ | ↓ |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | AF | |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | B0 | |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | B1 | |
| | | | ↓ | | | | | ↓ | ↓ |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | BF | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | C0 | |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | C1 | |
| | | | ↓ | | | | | ↓ | ↓ |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | CF | |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | D0 | |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | D1 | LC7501x series,LC7502x series (Audio DSP) |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | D2 | LC7501x series,LC7502x series (Audio DSP) |
| | | | ↓ | | | | | ↓ | ↓ |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | D7 | LC7505x series (Lip-sync surround) |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | D8 | LC7505x series (Lip-sync surround) |
| | | | ↓ | | | | | ↓ | ↓ |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | DF | |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | E0 | |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | E1 | |
| | | | ↓ | | | | | ↓ | ↓ |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | E8 | LC8905x series (DIR/DIT) |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | E9 | LC8905x series (DIR/DIT) |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | EA | LC8905x series (DIR/DIT) |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | EB | LC8905x series (DIR/DIT) |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | EC | LC8905x series (DIR/DIT) |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | ED | LC8905x series (DIR/DIT) |
| | | | ↓ | | | | | ↓ | ↓ |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | EF | |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | F0 | |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | F1 | |
| | | | ↓ | | | | | ↓ | ↓ |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | FA | LC7270x series (FMSS) |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | FB | LC7270x series (FMSS) |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | FC | LC7270x series (FMSS) |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | FD | LC7270x series (FMSS) |
| | | | ↓ | | | | | ↓ | ↓ |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FF | |

2. 4-bit address group

| CCB address | | | | | | | | | Device name (IC name) |
|---|---|---|---|---|---|---|---|---|---|
| Binary display LSB … MSB | | | | | | | | Hex display | |
| B0 | B1 | B2 | B3 | A0 | A1 | A2 | A3 | | |
| X | X | X | X | 1 | 0 | 0 | 0 | 1 | |
| X | X | X | X | 0 | 1 | 0 | 0 | 2 | |
| X | X | X | X | 1 | 1 | 0 | 0 | 3 | |
| X | X | X | X | 0 | 0 | 1 | 0 | 4 | LC7573F (VFD display driver) |
| X | X | X | X | 1 | 0 | 1 | 0 | 5 | LC7574F (VFD display driver) |
| ↓ | | | | | | | | ↓ | ↓ |
| X | X | X | X | 0 | 1 | 0 | 1 | A | LC78211 (Function switch) |
| X | X | X | X | 1 | 1 | 0 | 1 | B | LC78211 (Function switch) |
| X | X | X | X | 0 | 0 | 1 | 1 | C | LC78212 (Function switch) |
| X | X | X | X | 1 | 0 | 1 | 1 | D | LC78212 (Function switch) |
| X | X | X | X | 0 | 1 | 1 | 1 | E | LC78213 (Function switch) |
| X | X | X | X | 1 | 1 | 1 | 1 | F | LC78213 (Function switch) |

[Note] For serial data communication in 8-bit units, dummy data must be added to CCB addresses B0 to B3.
For serial data communication in 4-bit units, the data in CCB addresses B0 to B3 need not be transferred, but if ICs in the 8-bit address group and ICs in the 4-bit address group are to be connected on the same bus line, dummy data must be added to CCB addresses B0 to B3.



This catalog provides information as of October, 2008. Specifications and information herein are subject to change without notice.